23.4 A 1.4V 25mW Inductorless Wideband LNA in 0.13µm CMOS

Rashad Ramzan, Stefan Andersson, Jerzy Dabrowski, Christer Svensson

Linköping University, Linköping, Sweden

In recent years, the wireless communication has evolved towards multi-function and multi-standard terminals. Reducing the number of external components and the reuse of both digital and RF functional blocks is a key feature when a single terminal has to process a multitude of standards with different data rates, modulation types, and frequency bands. Usually, the requirement for low-cost in consumer electronics implies the use of CMOS technology. CMOS is well suited for high integration however the design of RF circuits in CMOS is challenging. The recent chipsets for multi-standard RF applications mainly use multiple narrowband or tunable LNAs [1]. These types of LNAs occupy larger chip real estate. High-Q inductors do not easily lend themselves for integration in a digital CMOS process, due to the need of special process enhancements such as high substrate resistivity to implement them. The CMOS process with RF enhancements usually lags one to two generations behind the digital one. The design migration of a system with RF blocks to a new process becomes very daunting due to the continuous scaling of CMOS technology.

In this paper, an inductorless wideband LNA implemented in a 0.13µm digital CMOS (without special RF enhancements) is proposed that is suitable for low-voltage operation. The differential LNA employs a current reuse technique to reduce the voltage drop across the load resistor and at the same time to improve the gain, noise performance, and power consumption. A common-drain stage in the feedback path is used to achieve 50Ω wideband input matching and partial noise cancellation at the same time. In measurements, the LNA achieves 17dB voltage gain (including output buffer with loss of 1.72dB), 7GHz bandwidth, 2.4dB NF at 3GHz, IIP3 and P_{1dB} of –4.1dBm and –20dBm, respectively. The measured power consumption excluding the output buffer is 25mW. The active area occupied by LNA and buffer is only 0.019mm^2.

The LNA schematic is shown in Fig. 23.4.1. In its forward path a cascode common-source stage is used where both M1 and M5 amplify the input signal. The bias current of PMOS transistor M5 is reused in NMOS transistor M1. Furthermore, connecting the gate of M5 to the input (using C_{C2}) also adds to the overall gain. Another advantage of M5 is a reduced voltage drop across the load resistor R_D that assures M1 and M4 to operate in saturation even for strong input signals and a low supply voltage. Consequently, a high-ohmic value of R_D can be laid out occupying a smaller chip area due to the reduced current. In addition, the associated parasitic capacitance, which tends to limit the BW and stability margin, is kept low. LNAs with negative feedback encircle several poles in the feedback loop and might become unstable at high frequency [2]. Therefore, the proposed LNA is carefully simulated for unconditional stability.

The gain, input impedance, and noise factor for a single-ended version of the LNA (assuming perfect input match) can be estimated with formulas shown in Fig. 23.4.5. The common-drain feedback stage consisting of M2 and R1 provides wideband 50Ω impedance match (100Ω differential) without a significant effect on the LNA voltage gain (*cf.* Eq(1)). By using this technique, the gain and NF can be selected independently of the input impedance, as opposed to the simple resistive shunt-series feedback LNA [3]. The approximate input impedance is given by Eq(2).

The cross-coupling capacitors C_{BW} between the input and the drain of M1 and M5 partly neutralize the input parasitic capacitance. This improves the bandwidth and the input matching at high frequency.

The main sources of noise are the channel noise of transistors M1, M2, M3, and M5. To calculate the NF and highlight the noise-cancellation mechanism, consider a simple model shown in Fig. 23.4.2. The channel thermal noise $\overline{I_n^2}$ of the input transistor produces a noise voltage $\overline{V_n^2}$ at the output. A scaled and bandlimited version of this noise is fed back to the gate of M1, where it is amplified and inverted. As a result, at the output (summing node), some of this correlated noise is cancelled and the total output noise is reduced (*cf.* Eq(3)). Without feedback, this noise voltage reduces to the well-known expression $\overline{V_{ni}^2} = 4\gamma_1 kT/g_{m1}$. Similarly, the channel noise of transistors M2, M4, and M5 is partially cancelled [1,3]. The level of cancellation depends upon the gain and impedance of the feedback path as well as the location of the noise source. The noise factor for a single-ended version of the input stage of LNA can be estimated from (*cf.* Eq(4)). The major noise contribution comes from M1 and M3. The latter one is outside the feedback loop and its noise is not subjected to the cancellation mechanism. Specifically, the noise contribution of M3 (10µm/0.26µm) is $(1 + g_{m2}.R_1)^2$ times larger than that of the feedback transistor M2 (5µm/0.13µm), since they have the same bias current and W/L ratio, resulting in $\gamma_3 g_{m3} \simeq \gamma_2 g_{m2}$ (*cf.* Eq(4)).

To improve IP3 of the LNA, the main input transistor M1 is biased at the optimum gate-source voltage of 360mV with I_D = 8mA and W/L = 200µm /0.13µm. At this bias point, the 3rd-order derivative of the DC characteristic is zero [4]. It crosses the zero line with a steep slope, which requires the bias voltage to be controlled precisely.

The RF signal at the gate of M2 can be large in amplitude rendering M2 to behave nonlinear. Resistor R1 mitigates this effect by providing a negative feedback for M2 that improves the linearity of the feedback path and hence the overall IP3.

The LNA is intended to drive an RF sampling front-end with two switched-capacitor decimation filters (I and Q), where the signal is sampled on four unit capacitors each with the value of 75fF. A DC-coupled differential source follower is used to drive this heavy capacitive load. A similar source-follower is used to drive the 50Ω off-chip load for measurement purposes. The bulk of the source-follower is connected to the source taking advantage of the triple-well process. The resulting voltage gain of the buffer is 0.82V/V at 2.4GHz.

The S-parameters are measured within 1-to-8GHz range. Hybrids are used to convert the single-ended signal from the network analyzer to a differential signal needed at the input of the LNA and vice versa with the output signal. The voltage gain, S_{11}, and S_{22} plots are shown in Fig. 23.4.3. The chip is bonded directly onto the PCB. Due to the physical area constraints of the board, it is not possible to layout continuous 50Ω tracks from SMA connector to the chip footprint. The pad capacitance of the SMA connectors and the pad capacitance of the chip footprint on the board, together with other board parasitics and mismatches, seem to be responsible for the uneven plots of the gain, S_{11} and S_{22}. The measured P_{1dB} (–20dBm) and IIP3 (–4.1dBm) are plotted in Fig. 23.4.4. Due to the limited capability of the measurement setup, the NF could only be measured in the range of 1 to 3GHz. The averaged NF is 2.7dB which is 0.4dB higher than simulated.

The performance of this LNA is comparable to other LNAs reported in the recent literature (Fig. 23.4.6), but is achieved with smaller supply voltage, area, and power.

References:

[1] S. Andersson, O. Drugge, and C. Svensson, "Wideband LNA for a Multistandard Wireless Receiver in 0.18µm CMOS," *Proc. ESSCIRC*, pp. 655-658 , Sept., 2003.

[2] J. Janssens, M. Steyaert, and H. Miyakawa,, "A 2.7-V CMOS Broadband Low-Noise Amplifier," *Symp. VLSI Circuits Dig. Tech. Papers,* pp. 87-88, June, 1997.

[3] F. Bruccoleri, E.A.M. Klumperink, and B. Nauta, "Wide-band CMOS Low-Noise Amplifier Exploiting Thermal-Noise Canceling," *IEEE J. Solid-State Circuits*, vol. 39, pp. 275-282, Feb., 2004.

[4] V. Aparin, G. Brown, and L.E. Larson: "Linearization of CMOS LNA's via Optimum Gate Biasing," *IEEE ISCAS*, pp. 748-751, May, 2004.

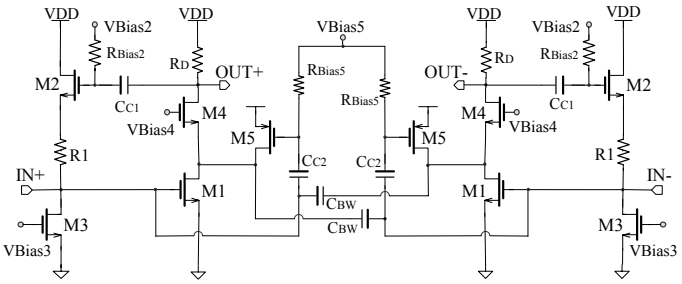

Figure 23.4.1: Differential input stage of the wideband LNA.

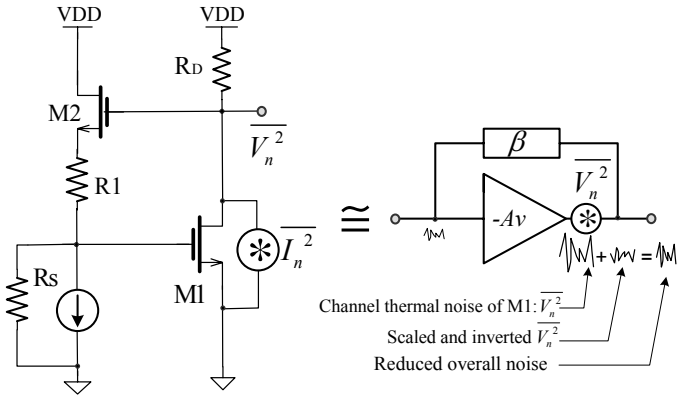

Figure 23.4.2: Simplified LNA model to highlight the partial thermal-noise cancellation of the input transistor M1.

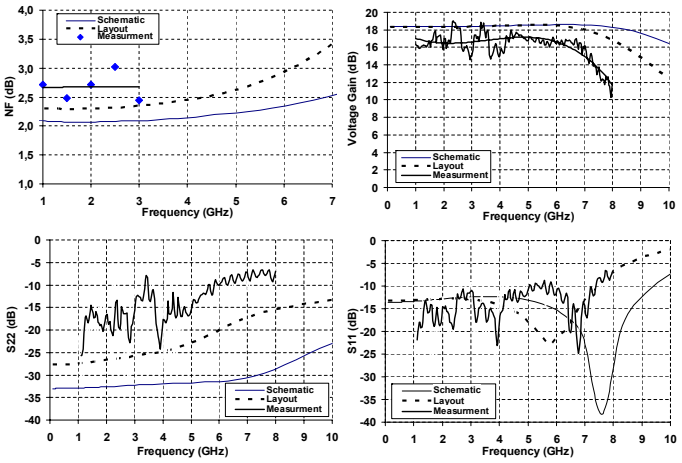

Figure 23.4.3: Measured and simulated NF, Gain, S_{22} and S_{11} performance.

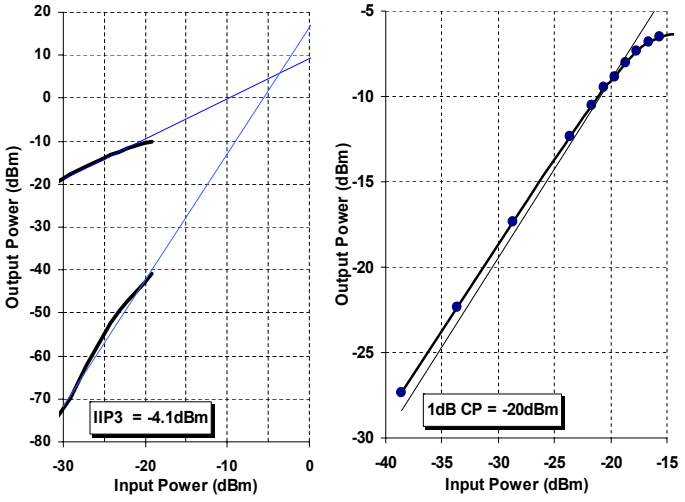

Figure 23.4.4: Measured IIP3 and P_{1dB}.

$$A_v = -\frac{(g_{m1}+g_{m5})g_{m4}.R_D}{(g_{m4}+g_{ds1}+g_{ds5})} = -G_m R_D \quad (1)$$

$$Z_{in} = \frac{1+g_{m2}R_1}{g_{m2}(1+G_m R_D)} = \frac{1+g_{m2}R_1}{g_{m2}\left(1+\left|A_v\right|\right)} \quad (2)$$

$$\overline{V_{ni}^2} = \frac{kT.\gamma_1}{g_{m1}}.\left(1+\frac{1}{1+\left|A_v\right|}\right)^2 \quad (3)$$

$$F = 1+\left(1+\frac{1}{1+\left|A_v\right|}\right)^2\left(\frac{\gamma_1}{4g_{m1}R_s}+\frac{\gamma_5}{4g_{m5}R_s}\right)+\frac{\gamma_3 g_{m3}R_s}{4}+ \frac{\gamma_2 g_{m2}R_s}{4\left(1+g_{m2}R_1\right)^2}+\frac{R_1}{4R_s\left(1+\left|A_v\right|\right)^2}+\frac{R_D}{4R_s\left(1+\left|A_v\right|\right)^2} \quad (4)$$

where γ_1, γ_2, γ_3 and γ_5 are the noise coefficients of M1, M2, M3 and M5, respectively

Figure 23.4.5: Circuit equations.

Source	Process	Freq (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Supply (V)	Power (mW)	Active Area (mm^2)
This Work	130nm CMOS	1-7	17	2.4	-4.1	1.4	25	0.019
ISSCC 2006 pp. 200	90nm CMOS	0.5-8.2	25	1.9-2.6	-4	2.7	42	0.025
JSSC 2005 pp. 544	180nm CMOS	2-4.6	9.8*	2.3	-7	1.8	12.6	0.9
JSSC 2004 pp. 2269	180nm SiGe BiCMOS	3-10	21*	2.5-4.2	-1	3	30	0.7
JSSC 2004 pp. 2259	180nm CMOS	2.3-9.2	9.3*	4	-16	1.8	9	0.66
ESSCIRC 2003 pp. 655	180nm CMOS	1-7	13.1*	3.7	-4.7	1.8	75	0.18

* Power Gain

Figure 23.4.6: Performance summary and comparison.

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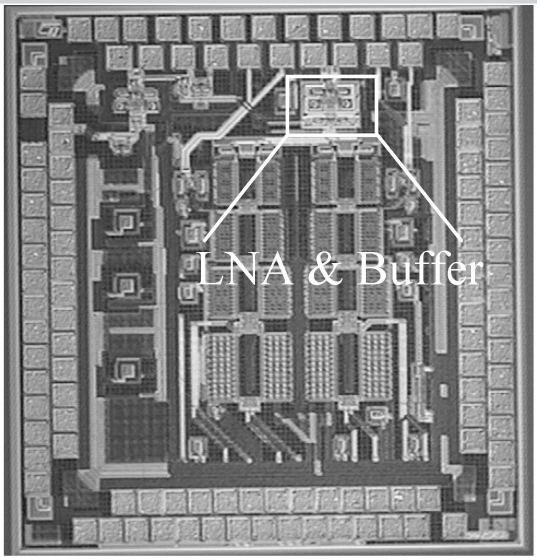

Figure 23.4.7: Chip micrograph.

